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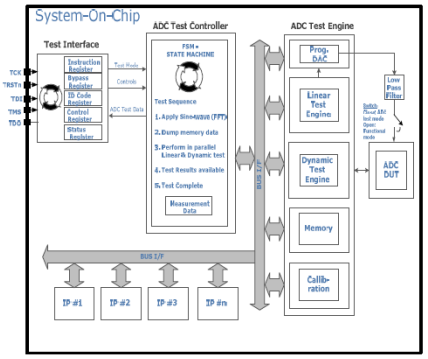
Licensing Opportunity: Programmable on-chip ADC Test Solution

Overview



Example SoC design incorporating ADC BIST

Mixed-signal System-on-Chip (SoC) testing has become prohibitively expensive with the ever increasing integration of complex analogue circuitry. Specifically, data converters are components that require significant test resources. University of Limerick researchers have developed, patent protected, technology that allows SoC developers and Analogue-Digital Converters (ADC) IP vendors to easily embed Built-in-Self-Test (BIST) logic targeted at ADC devices. A mostly digital platform is easily incorporated to completely self-test the ADC device and deliver measurements such as linearity and dynamic responses

Technology

The BIST solution is accessible via the IEEE 1149.1 JTAG interface to initiate ADC test and measurement with results available to any low-cost ATE tester. The technology incorporates three significant IP blocks in the form of a programmable Digital-Analogue Converter (DAC) that provides an accurate signal waveform into the Linear (LTE) and Dynamic Test Engine (DTE) blocks. These modules operate independently and can perform linear and dynamic ADC measurement in parallel to minimize ADC test time and more importantly test cost. This technology enables a complete on-chip solution to ADC testing that can be activated not only during production test but also can be reused for in-situ ADC calibration and debug. The IP blocks can also be re-deployed functionally for user- specific application when testing is not required.
The integrated IC test system has many benefits for enabling on-chip ADC design for test (DFT) and debug (DFD) potential.

Test Costs: The technology offers a low-cost replacement to the traditional expensive mixed-signal ATE route by dramatically reducing test time and eliminating DUT probe design and complicated test setup requirements. The mixed-signal testing is reduced to a simple digital go/no-go response.

Test Accuracy: The system is a self-contained on-chip solution using the JTAG interface to initiate test and access results. No other external probe cards and ATE interfacing are required thereby minimizing external noise influences leading to improved results accuracy and better reliability.

Integration Ease: Digital designs are easily integrated using typical IC design flows while FPGA prototyping before silicon manufactures gives confidence to the total technology solution.

Digital IP Solution: A digital test solution for mixed-signal ADC devices is less complicated to integrate and facilitates lower test costs on a digital test platform. IP such as the programmable sigma-delta DAC and Dynamic Test Engine - an optimal CPU architecture can be easily redeployed functionally for other user applications. Logic reuse maximises the functionality of the hardware on-chip while minimizing the logic overheads and reducing costs further.

Debug Capability: The ADC metrics can be checked in production test to help improve yield diagnostics and to determine ADC datasheet performance while operating in-situ. Errors can be quickly diagnosed and corrected using self-calibration by effecting gain and offset values. Test debug can isolate issues in the field leading to increased reliability and lower down time

Commercial Opportunity

The University of Limerick is interested in seeking partners to exploit the commercial potential of these technologies by entering into licensing and collaboration agreements that mutually benefit both parties.

IP Status

A patent for this intellectual property has been granted, US 8386209.

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